LIFE CYCLE ASSESSMENT FOR RAPIDLY EVOLVING TECHNOLOGIES

A CASE STUDY ON GLOBAL INTEGRATED CIRCUIT MANUFACTURING

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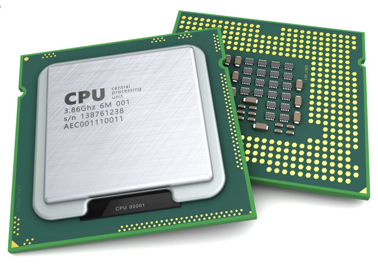
OVERVIEW [1,2,3]

- Information & Communication Technology (ICT) contributes 2-4% of global greenhouse gas emissions.
- Scope 3 upstream emissions can contribute 30-90% of total ICT emissions, depending on the product category.
- Integrated circuits are key contributors to upstream scope 3 emissions of data centers and computing systems.
- Companies are committing to reducing ICT emissions from upstream scope 3 but limited LCA data exists.



LCA DATA CHALLENGES

- Rapidly evolving products with wide variation in product category complexity
- Highly proprietary processing & ingredient information [4,5]
- Literature data from early 2000's
- Databases assume linear scaling properties but ignore nonlinear changes in processing technologies and complexity

LCA DATA LIMITATIONS

- Data limited to specific geographies, processing tech
- Unaccounted nonlinearities
- Uncertainties in mitigation opportunities
- Difficult to compare across LCAs: minimal transparency and variable system boundaries and assumptions

Poses signficant challenges for accurate product LCA, scope 3 measurement and mitigation

GOAL & SCOPE

Develop a parameterized, streamlined LCA to explore potential variation in semiconductor cradle-to-processing gate emissions across product types, product generations, regional production contexts, product technologies and design to identify potential levers for mitigating GHG emissions.

DESIGN SCENARIO PARAMETERS

Simulation Model Scenario Parameters

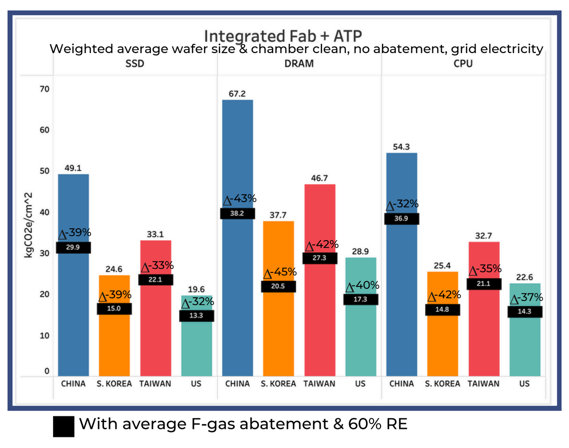
- **Fab size:** [150-200mm, 300+mm]
- **Country of production:** [China, South Korea, Taiwan, US]
- **Product type:** [DRAM, SSD, CPU, GPU]
- **Technology type:** [In situ thermal clean, In situ plasma clean, Remote plasma clean]
- **Gas replacement:** [F2, C3F8, C4F8O, C4F8]
- **Electricity management:** [Renewables, Efficiency, grid decarbonization]
- **Generation node:** [90nm, 60nm, 40nm, 28nm, 20nm, 16nm, 10nm, 7nm, 5nm]
- **Fabrication design details:** [Deck stacking: single, 2D, 3D, 4D]
- **Assembly design details:** [Die stacking], [chips per package], [die size], [bit or transistor density], [defect density]
- **Abatement technology/adoption:** [combustion, hot-wet (electrical), plasma, catalytic]

Baseline default design assumptions

Parameters	SSD	DRAM	CPU
Node Generation	20nm	20nm	20nm
Capacity per Package	633 Gb	6 Gb	5,776 MTr
Deck Stacking	3D	2D	2D
Wafer Mask Layers	97	101	124
Size of die	118 mm2	53 mm2	312 mm2
Die per Wafer (200mm)	225	530	76
Die per Wafer (300mm)	537	1238	189
Bit or Transistor Density	5.4 Gb/mm2	0.1 Gb/mm2	19 MTr/mm2
Die stacking	1	1	1
Chips per Package	1	1	1
Defect Density (#/cm2/die)	0.1	0.1	0.1
Yield	89%	95%	74%

EMISSIONS INTENSITY

GHG Emissions & Mitigation Opportunities vary by product category & country

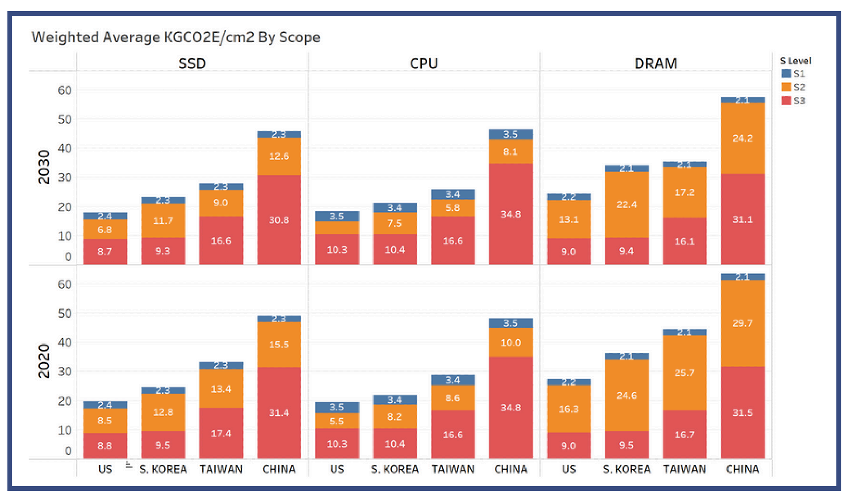


REDUCTION POTENTIAL

- SSD 32-39%
- DRAM 40-45%
- CPU 32-42%

Scope 2 emissions are biggest single hotspot

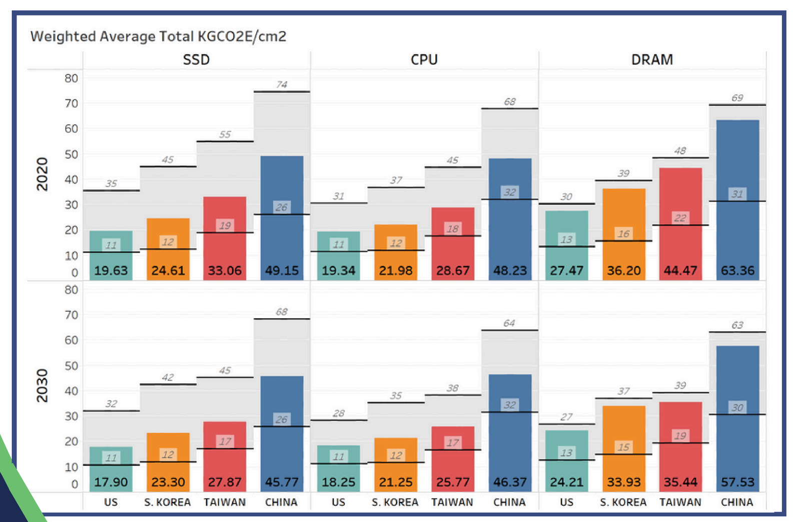
Scope 3 emissions vary by country and are a significant proportion of total emissions in aggregate



EXAMPLE RANGE OF SIMULATED PRODUCTION POSSIBILITIES

2020 grid vs. 2030 grid decarb
0-100% Renewable energy adoptions
~16-20nm (default design parameters)
0-100% F-gas abatement across tech types

Product types
Technology types
Grid mix & projections
Country of production
Wafer size (200 vs. 300mm)



LEVERAGE POINTS

Renewable Energy
300mm Wafer Sizes
SBTi Upstream Targets
Remote Plasma Clean
F-Gas Abatement

GHG MITIGATION OPPORTUNITIES

METHODS [6]

Identify hotspots through initial scoping analysis
Fabrication | Assembly, Testing, Packaging (ATP)

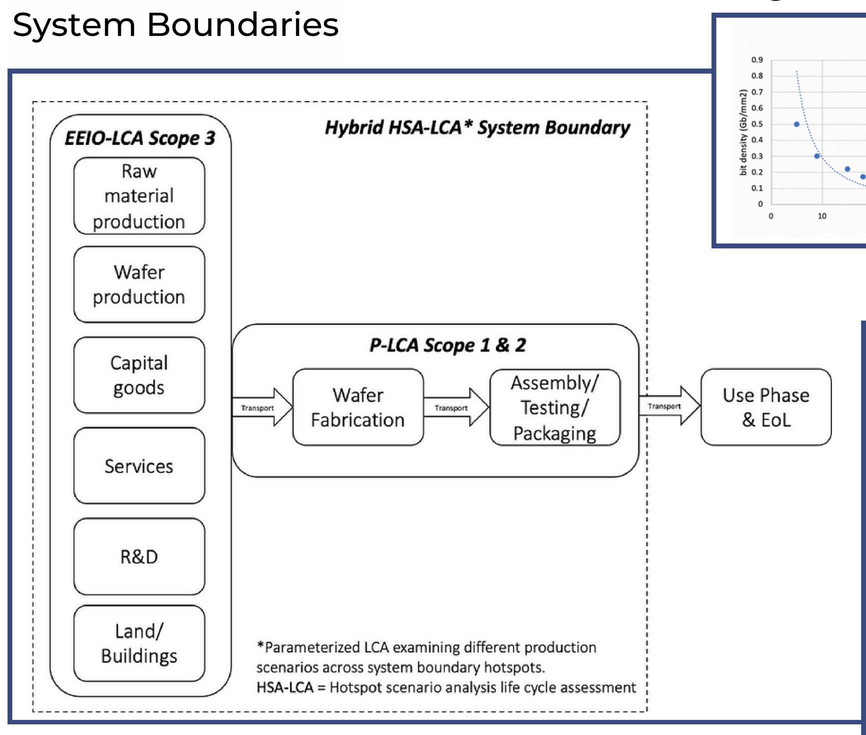
2) Develop parameterized LCI within hotspot stages
Govt Reports | Public Data | Regression Analysis of Gaps

3) Use general LCA information for non-hotspots
EEIO | Existing PLCA's Reflecting Industry Averages

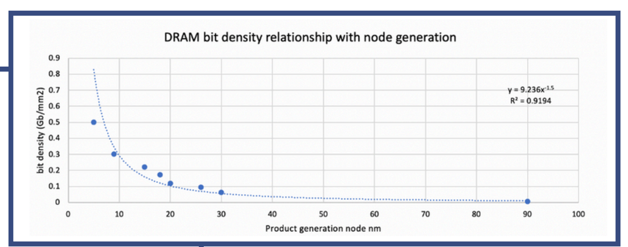
4) Identify key parameter levers affecting hotspot impacts
Literature | Iterative Model Building | Sensitivity Analysis

5) Simulate discreet scenario permutations & estimate mitigation potential
Capture dynamics across combinations of scenarios

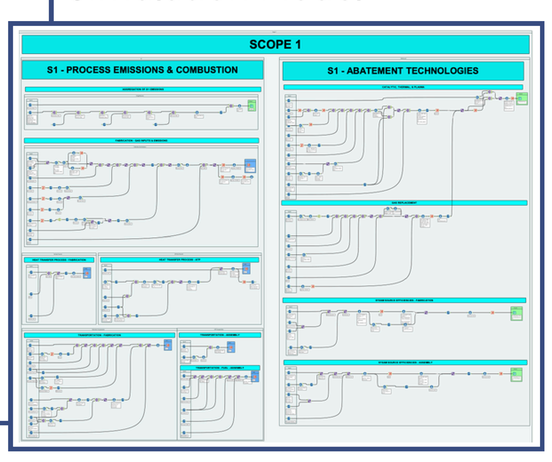
System Boundaries



Regressions for filling data gaps



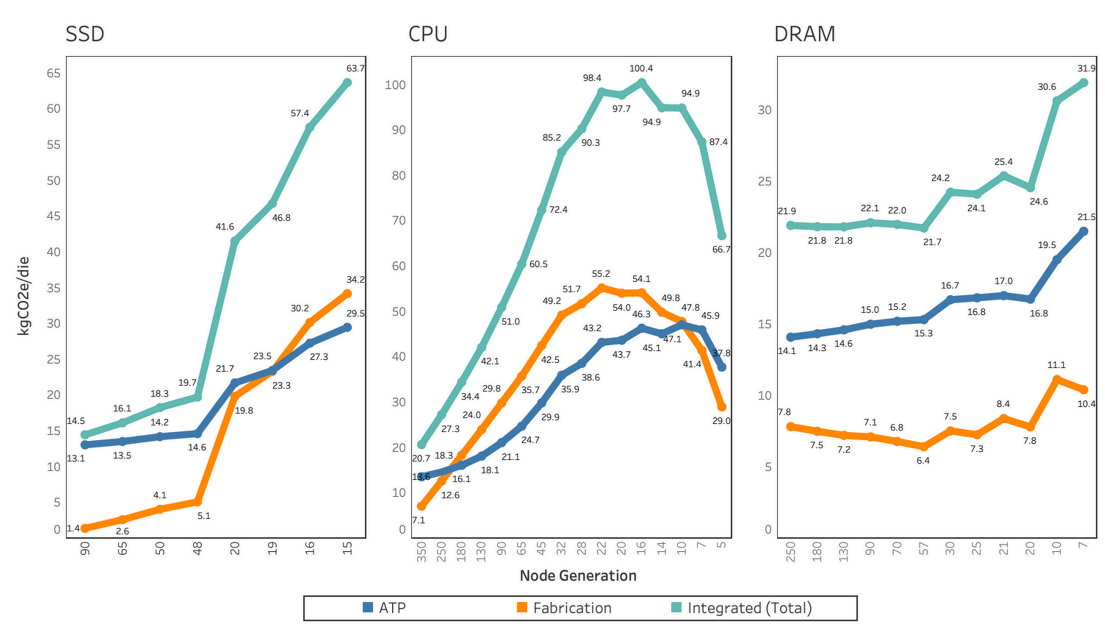
Simulation Model



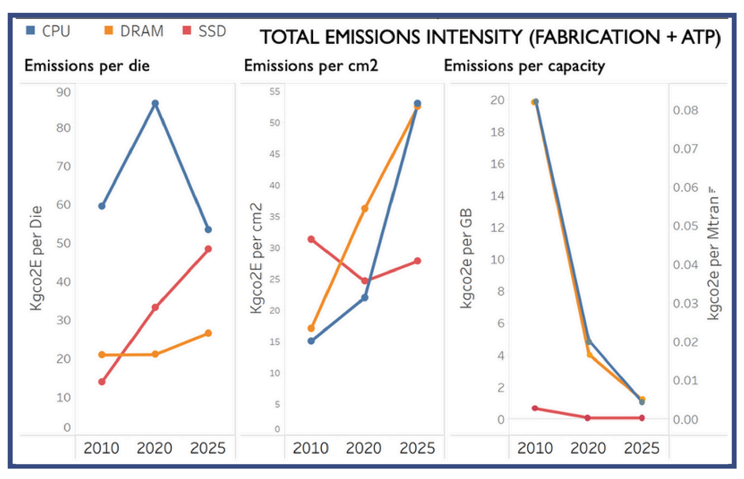
SIMULATION DYNAMICS

Relative contribution from ATP vs. Fabrication production stages depends on product type and tech generation, having implications for supply chain engagement targets for how far to reach up the supply chain to effectively reduce emissions.

GHG Contributions Change across Tech Gens



GHG Trends Change across functional units



Emissions Intensity trends depend on the chosen functional unit, with implications for target setting:

- Generally increasing GHG per die & per cm^2 in newer generations
- Decreasing GHG per storage or processing capacity for newer product generations

Simulation Considerations:

- Product types
- Electricity
- Die size (mm2)
- Node generations
- Wafer mask layers

BENEFITS OF PARAMETERIZED LCA

- Increase comparability across production & sourcing scenarios, avoiding inconsistent system boundaries, allocations, functional units, & other differences in assumptions.
- Enables prospective modeling for examining alternative production scenarios & mitigation options with enhanced comparability for directionally consistent decision signals.
- Reduces costs of analysis through parameterization & prioritizing high impact components of supply chain, which maintains comprehensiveness of the broader system.
- Increases timeliness & actionability of information for setting climate action plans & achieving targets.

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